US-PAT-NO: 6664482

DOCUMENT-IDENTIFIER: US 6664482 B1

TITLE: Printed circuit board having solder bridges for electronically connecting conducting pads and method of fabricating solder bridges

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Brief Summary Text - BSTX (5):

In typical surface mounting processes, a solder paste is applied to the conducting pads of the PCB blank through a stencil patterned with openings corresponding to the PCB blank conducting pad locations. Typically, the solder paste is screen deposited onto the conducting pads using the **stencil as a mask and a blade to squeegee the solder paste through the holes in the stencil**. When the stencil is removed, the solder paste remains on the conducting pads of the PCB blank. Next, the leads of the electrical components are placed on the soldered conducting pads, and the solder paste is subjected to reflow soldering to adhere the leads to the conducting pads. To prevent solder shorts (i.e., the unwanted formation of an electrical connection between conducting pads), due to the imprecise application of the soldering paste or the unwanted flow of solder during the reflow soldering process, the conducting pads are often fabricated on the PCB blank so as to have an edge-to-edge conducting pad separation of between 20-100 mils with a minimum edge-to-edge conducting pad separation of at least 12 mils.

Brief Summary Text - BSTX (15):

In still another embodiment, the present invention provides a stencil device for insuring that solder paste is accurately applied to a printed circuit board

during routine handling, nor is it susceptible to becoming dislodged or inadvertently misaligned during the printed circuit board manufacturing process. Moreover, since the zero signal degradation solder bridge electrical connection forms a short, direct electrical connection between the conducting pads, degradation of the integrity of the electrical signal and parasitic capacitance and inductance between connected conducting pads is minimized especially when compared to the separate electrical components referred to above. Further, it is relatively easy to reconfigure the printed circuit board during the manufacturing process since the reconfiguring of any zero signal degradation electrical connections only requires modification of the **stencil which may in some instances be accomplished simply by masking off with tape unwanted solder bridge connections on the stencil**. Lastly, these substantially zero signal degradation electrical connections are rotatable through any angle so as to be mountable to the printed circuit board at any angle (not just 90.degree. and 180.degree.) to allow the printed circuit board to employ various conducting pad geometries and groupings to take advantage of available printed circuit board surface space.

Drawing Description Text - DRTX (10):

FIG. 8 is a top elevational view similar to FIG. 7 of the **stencil with an opening masked** off with tape.

Detailed Description Text - DETX (9):

As seen in FIG. 7, the stencil plate member 44 also defines a **second opening** 52 having a first open portion 54 sized to substantially correspond to the third conducting pad 26, a second open portion 56 sized to substantially correspond to the fourth conducting pad 28 and a third open portion 58 that links the first open portion 54 to the second open portion 56 and is sized to

correspond to a partial portion of the surface area 34 of the first surface 14 between the edges 30, 32 of the third and fourth conducting pads 26, 28, such that upon application of solder paste 46 to the stencil plate member 44, the solder paste 46 flows through the first, second and third open portions 54, 56, 58 of the **second opening** 52 and onto the third and fourth conducting pads 26, 28 and the first surface 14 of the dielectric structure core 12 to form the substantially zero signal degradation electrical connection 42 between the third and fourth conducting pads 26, 28.

Detailed Description Text - DETX (10):

As seen in FIG. 8, it is relatively easy to reconfigure the printed circuit board product 10 during the manufacturing process since the reconfiguring of any substantially zero signal degradation electrical connections 36, 42 only requires modification of the **stencil 44 which may in some instances be accomplished simply by masking** off with tape 60 unwanted solder bridge connection openings (such as solder bridge connection opening 52) on the stencil 44.

Detailed Description Text - DETX (11):

In practice, as illustrated in FIG. 10, the substantially zero signal degradation solder bridge electrical connections 36, 42 are fabricated using the following method. First, as represented by reference numeral 62, a printed circuit board product 10 defined by a dielectric structure core 12 having a first surface 14, conducting pads 18-28 having adjoining edges 30, 32 that define therebetween a surface area 34 of the first surface 14 is provided. Next, as represented by reference numeral 64, if desired unwanted solder bridge fabricating openings 50, 52 in the **stencil plate member 44 can be masked** off using a piece of tape 60 to prevent solder paste from flowing through the these

openings and onto select conducting pads 18-28. If it is not necessary to modify the printed circuit board product 10, then this step 64 is simply omitted and fabrication proceeds with the next step 66. In step 66, the stencil 44 is placed on the first surface 14 of the dielectric structure core 12 with the solder bridge fabricating openings 50, 52 aligned with the appropriate conducting pads 18-28. In this example, the fabricating opening 50 would be aligned with the first and second conducting pads 18, 20, and the fabricating opening 52 would be aligned with the third and fourth conducting pads 26, 28.

Detailed Description Text - DETX (13):

The method of fabricating the substantially zero signal degradation solder bridge electrical connections 36, 42 for connecting conducting pads 18-28 of the printed circuit board product 10, and the printed circuit board 10 having at least one of these solder bridges 36, 42 in accordance with the present invention do not require the use of separate electrical components (such as "zero ohm resistors", "dip switches" and "header array/jumper blocks"). As such the cost of fabricating such a printed circuit board 10 is reduced. In addition, since this substantially zero signal degradation solder bridge electrical connection 36, 42 has such a low profile, it is not susceptible to damage during routine handling, nor is it susceptible to becoming dislodged or inadvertently misaligned during the printed circuit board manufacturing process. Moreover, since the substantially zero signal degradation solder bridge electrical connections 36, 42 form a short, direct electrical connection between the conducting pads 18-28, degradation of the integrity of the electrical signal and parasitic capacitance and inductance between connected conducting pads is minimized especially when compared to the separate

electrical components referred to above. Further, it is relatively easy to reconfigure the printed circuit board 10 during the manufacturing process since the reconfiguring of any substantially zero signal degradation electrical connections only requires modification of the **stencil 44 which may in some instances be accomplished simply by masking** off with tape 60 unwanted solder bridge fabrication openings 50, 52 in the stencil 44. Lastly, these substantially zero signal degradation electrical connections 36, 42 are rotatable through any angle so as to be mountable to the printed circuit board 10 at any angle (not just 90.degree. and 180.degree.) to allow the printed circuit board 10 to employ various conducting pad geometries and groupings to take advantage of available printed circuit board surface space.